**California State University, Northridge**

**College of Engineering & Computer Science**

**Electrical and Computer Engineering Department**

**ECE 443L Digital Electronics Laboratory Report 7**

**CMOS based Sample and Hold Circuit Design, Simulation and Experimental Test as well as Analysis**

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**Abstract:**

A sample and hold circuit samples an analog input voltage at a certain point in time and holds the sampled voltage for an extended time after the sample is taken. A sample and hold will keep the sampled analog voltage constant for the length of time necessary to allow an analog to digital converter (ADC) to convert the voltage to a digital form. A basic sample and hold circuit consist of an analog switch, a capacitor, and I/O- Amplifiers.

Diagram

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Basic Sample and hold circuit

**Sample and hold specifications:**

* Aperture time- the time for the analog switch to fully open after the contro voltge switches from its sample level to its hold level.
* Aperature jitter- the uncertainty in the aperature time
* Acquisition time – the time required for the device to reach its final value when the control voltage switches from its hold level to its sample level
* Droop – the change in voltage from the sampled value during the hold interval because of charge leaking off of the hold capacitor
* Feedthrough – the component of the output voltage that follows the input signal after the analog switch is opened. The inherent capacitance from the input to the output of the switches causes feedthrough

Diagram

Description automatically generated

**Author 1 Case 1, 3, and 5:**

Diagram, schematic

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Case 1 @ 5kHz with 11Mega Ohm resistor and 160pF capacitor

Chart, line chart

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Table

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Case 1 output when using the components from circuit

Diagram, schematic

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Case 3 circuit with 100pF capacitor and 100 Meg resistor running at a frequency of 30kHz

Chart

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Table

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Case 3 waveform using the above components.

Diagram, schematic

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Case 5 Ramp circuit with a period of 33 micro seconds or about 30kHz and a .01pF capacitor paired with 50 ohm resistors.

Chart, line chart

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Table

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Discharge of the capacitor seems to stay constant and cannot match the ramp circuit perfectly.

**Author 2 Case 2, 4, 6:**

**Experimental Results:**

Chart, histogram

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Chart, histogram

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Chart

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**Author 1 Alternate case 1, 3, and 5:**

Diagram, schematic

Description automatically generated

Fig 7.1 Sample and Hold Circuit, fin = 5kHz and fclk = 100khz.

Chart, line chart

Description automatically generated

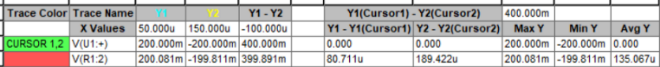


Fig 7.2 Sample and Hold simulation results, fin = 5kHz and fclk = 100khz.

Diagram, schematic

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Fig 7.3 Sample and Hold Circuit, fin = 40kHz and fclk = 600khz.

Chart

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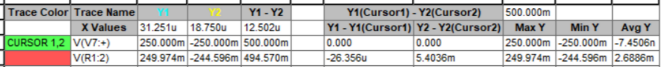


Fig 7.4 Sample and Hold simulation results, fin = 40kHz and fclk = 600khz.

Diagram, schematic

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Fig 7.5 Sample and Hold Circuit, fin = 5kHz Ramp case and fclk = 33khz.

Chart, line chart

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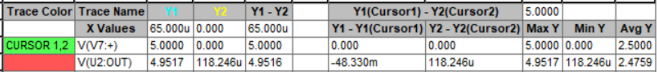


Fig 7.5 Sample and Hold simulation results, fin = 5kHz Ramp case and fclk = 33khz.

**Conclusion:**

In this lab we were able to simulate and experimentally show how a sample and hold circuit works.